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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,659	04/02/2004	Gregory J. Wilson	63857.8157.US04	3413

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PERKINS COIE LLP/SEMITOOL
PO BOX 1208
SEATTLE, WA 98111-1208

EXAMINER	
SMITH, NICHOLAS A	

ART UNIT	PAPER NUMBER
1795	

MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,659	WILSON ET AL.	
	Examiner	Art Unit	
	NICHOLAS A. SMITH	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *104-108,110,111,120,128-130,132 and 134-144* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *104-108,110,111,120,128-130,132 and 134-144* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/7/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 104-108,110,111,120,128-130,132 and 134-144 is withdrawn in view of the newly discovered reference(s) to Japanese Unexamined Patent Publication H07-197299 as submitted on 7 August 2008 in Applicant's Information Disclosure Statement. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 104-105,110,120,128-130,132 and 134-140 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Unexamined Patent Publication H07-197299 translation as submitted on 7 August 2008 in Applicant's Information Disclosure Statement.

4. In regards to claim(s) 104-105, 108, 110, 120, 128-130, 132 and 134-140, JP'299 discloses a method of and a computer-readable medium capable of causing a computer system to adjust currents for a plurality of electrodes in an electroplating chamber to improve plating uniformity by obtaining a plating thickness on the workpiece at that radius when a set of baseline currents are delivered through the electrodes (Figs. 3 and 6), obtaining for each electrode a plating thickness on the workpiece at that radius when

the baseline currents are perturbed for that electrode (paragraph [0026], key input portion **48** and CPU **47**), and then calculating the proper current adjustments to make a uniform height (i.e. a target profile) over the entire distribution of the wafer (paragraph [0026]). While JP'299 does not explicitly disclose a matrix, the matrix is inherently in JP'299's computer system; a matrix of thicknesses and current applied for each electrode is necessary to make the calculation as disclosed in paragraph [0026] in order to improve plating uniformity and control of current adjustments, therefore, such a matrix is inherent in JP'299. Furthermore, calculations inherently provide a third set of parameters to provide a more uniform surface on a second workpiece after the first perturbation by key input portion **48** and CPU **47**. The key input portion **48** provides a simulation of the operation of the electroplating chamber. JP'299 is applied repetitively and under different conditions. Furthermore, it is noted that JP'299 indicates that uniformity variations occur from center to periphery of the wafer for variations in the manufacturing conditions for IC chips.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 106 and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP'299.

7. JP'299 discloses a range (0 to 100%) of changing the current applied that overlaps the claimed range and therefore establishes a case of prima facie obviousness. See MPEP 2144.05. It would have been obvious to one of ordinary skill in the art to select the claimed range of current changes from the broader prior art range because prior art teaches utility over the entire range.

8. Claims 111 and 141-144 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP'299 in view of Jorne et al. (US 6132587 A).

9. JP'299 teaches the limitations as stated above in paragraph 4.

10. However, JP'299 does not explicitly disclose that variations in the manufacturing conditions for IC chips are due to different seed layer conditions.

11. Jorne et al. teaches that seed layers conditions affect the uniformity (or non-uniformity) of the plating process (abstract). It would have been obvious to one of ordinary skill in the art to select Jorne et al.'s method of recognizing that seed layer conditions affect plating uniformity as a more specific indication of JP'299 of variations in manufacturing conditions for IC chips because there are a finite number of predictable variables for manufacturing conditions and there is a reasonable expectation of success. See MPEP 2141 III (E).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NICHOLAS A. SMITH whose telephone number is (571)272-8760. The examiner can normally be reached on 8:30 AM to 5:00 PM, Monday through Friday.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on (571)-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry D Wilkins, III/
Primary Examiner, Art Unit 1795

NAS